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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/729,907	12/09/2003	Kazunori Nozawa	056208.53057US	3294

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EXAMINER

RUTLAND WALLIS, MICHAEL

ART UNIT	PAPER NUMBER
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2836

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/11/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.		Applicant(s)	
	10/729,907		NOZAWA ET AL.	
	Examiner		Art Unit	
	Michael Rutland-Wallis		2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12/09/2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) 8-11 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☐ Claim(s) 1-7 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 09 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>12/09/2003 10/21/05</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 1 and 2-7 in the reply filed on 12/04/2006 is acknowledged.

Specification

The disclosure is objected to because of the following informalities: page 3 line 2 recites "VIGN voltage 3a is changed from the HI signal to the HI signal". Applicant should amend the above language to clearly state what signal change the CPU detects

Abstract

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The

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abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

At a minimum Applicant should remove subject headings in the abstract specifically in line 1 "(subject)" and line 11 "(Means for Solving the Problems)"

Claim Objections

Claims 1 and 2 recites the limitation "said OFF signal" in line 11. There is insufficient antecedent basis for this limitation in the claim.

Claim 4 recites "said delay circuit is a delay circuit constituted by..." said limitation is redundant and is suggest to be amended to "said delay circuit constituted by..."

Claim 7 is objected to as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 7 recites "and an AND circuit" as understood by the examiner this limitations should be changed to read "and the AND circuit". Further claim 7 recited "and another port signal of said central processing unit is installed". The installation of a first port signal of said

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central processing unit has not been recited. It is unclear what Applicant intends by the limitation another port signal of said central processing unit is installed.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 and 6-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshihara (JP No. 62-156063)

With respect to claim 1 Yoshihara teaches an electronic control unit for car comprising: a battery power source (item 6); an ignition switch (presence or absence of item 8 the ignition key see page 3 lines 5-11 or page 10 line 3 describing the opening of the ignition key); and a power source IC (item 5) for supplying a constant voltage (5VDC) to said electronic control unit (item 4) including a central processing unit (item b) when said ignition switch (item 8) is turned on and for interrupting said supply of said constant voltage when said ignition switch is turned off (item 8 removed or disconnected); characterized by comprising a delay circuit (item 12) for delaying said OFF signal (low-level opening instruction page 4 line 15) by a predetermined time (see time constant formed by item 13) when said ignition switch is turned off; wherein said

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supply of said constant voltage to said electronic control unit from said power source IC is interrupted (via switch circuit item 7) by an output signal of said delay circuit (item 12).

With respect to claim 2 Yoshihara teaches an electronic control unit for car comprising: a battery power source (item 6); an ignition switch (presence or absence of item 8 the ignition key see page 3 lines 5-11 or page 10 line 3 describing the opening of the ignition key); and a power source IC (item 5) for supplying a constant voltage (5VDC) to said electronic control unit (item 4) including a central processing unit (item b) when said ignition switch (item 8) is turned on and for interrupting said supply of said constant voltage when said ignition switch is turned off (item 8 removed or disconnected); characterized by comprising a delay circuit (resistor and capacitor circuitry item 13 coupled to transistor Q) for delaying said OFF signal (low-level opening instruction page 4 line 15) by a predetermined time (see time constant formed by item 13) when said ignition switch is turned off, an AND (item 14) circuit inputting (into switch circuit 7) an output signal (OFF signal) of said delay circuit, and inputting a constant voltage supply interruption signal generated by said central processing unit after a lapse of a predetermined time (after capacitor discharge falls below threshold of the logic level of the AND circuit) when said central processing unit detects interruption (removal or opening of key) of said power supply from said battery (item 6); wherein said supply of said constant voltage to said electronic control unit from said power source IC (item 5) is interrupted by an output signal of said AND circuit (item 14).

With respect to claim 3 Yoshihara teaches the (page 4 line 5-10) CPU is allowed to operate after the vehicle has stopped traveling and has been turned off, until the CPU terminates collection of the vehicle operation data.

With respect to claim 4 Yoshihara teaches said delay circuit (item 12) is a delay circuit constituted by a resistor (R), a capacitor (C), and a diode (D) and by selecting constants thereof, said delay time is set.

With respect to claim 6 Yoshihara teaches the use of a separate detection circuit (item 9), wherein the detection circuit is connected to the input of the controller and the CPU in order to communicate the interruption to the central processing unit. Yoshihara also teaches after a lapse of a predetermined time required for stop initialization (page 4 line 5-10) to an input port (seen connected to output of item 5) monitors for a power from the constant voltage

With respect to claim 7 Yoshihara teaches the use of a separate detection circuit (item 9), wherein the detection circuit is connected to the input of the controller and the AND circuit and the CPU in order to communicate the interruption to the central processing unit. Yoshihara also teaches after a lapse of a predetermined time required for stop initialization (page 4 line 5-10) to an input port (seen connected to output of item 5) monitors for a power from the constant voltage

Claim Rejections - 35 USC § 103

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The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshihara (JP No. 62-156063) in view of Toshihiko et al. (JP No. 59-176992) Yoshihara teaches the time circuit is formed using a resistor capacitor circuit, Yoshihara does not teach the use of a counter. Toshihiko teaches the use of a counter in the protection of a of battery discharge. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a counter in the system of Yoshihara in the place of a resistor capacitor in order to maintain a longer delay

Conclusion

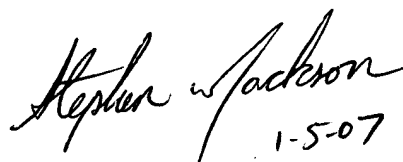
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Rutland-Wallis whose telephone number is 571-272-5921. The examiner can normally be reached on Monday-Thursday 7:30AM-6:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MRW



1-5-07

STEPHEN W. JACKSON
PRIMARY EXAMINER